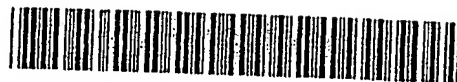


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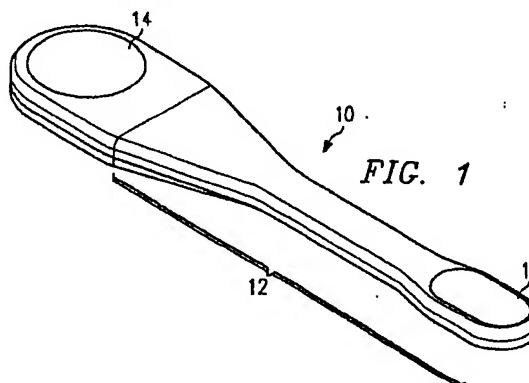
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(54) Implantable bone growth stimulator and method of operation.

(57) A method for the therapeutic stimulation of bone growth of a bone site is disclosed comprising the steps of implanting first and second electrodes into the tissue near the base site. The electrodes are coupled to a bone growth stimulator which generates an alternating current.



A second technical advantage of the invention is its AC nature. Because the device is AC, the electrodes may be placed away from the injury site, e.g. subcutaneously. This causes less trauma to the surrounding tissue during implant and ex-
plant, reduces the chances of infection and in-
creases imaging results. Further, the remote place-
ment requires no change in conventional orthope-
dic surgical procedures.

A third technical advantage of the device is its programmability. The operation of the device may be modified by an external transmitter/receiver dur-
ing its lifetime to better suit the needs of the
patient. A magnetic pulse is used to relay digital
signals to the stimulator.

A fourth technical advantage of the device is its monitorability. The device has the ability to monitor important characteristics of its operation and report these via a low frequency magnetic pulse to an
external device for an evaluation by a physician.
This insures maximum therapeutic value to the
patient. The patient can avoid wearing a defective
bone growth stimulator if such defect can be deter-
mined and remedied.

The final technical advantage of the device is the disclosed electrode structure. The electrodes are two flat conductive surfaces located on one
face of the disclosed stimulator. A physician may
implant the device such that the electrodes face
away from the underlying bone structure and sur-
rounding muscle mass. This has been shown to
increase the effectiveness of the stimulator.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying draw-
ings, in which:

FIGURES 1 and 2 are isometric illustrations of the disclosed bone growth stimulator configured for generating an alternating current output;

FIGURE 3 is an isometric illustration of the dis-
closed bone growth stimulator configured for
generating a direct current output;

FIGURE 4 is a graphical representation of the
output of the bone growth stimulator depicted in
FIGURES 1 and 2;

FIGURE 5 is a graphical representation of the
output of the bone growth stimulator depicted in
FIGURE 3;

FIGURE 6 is a simplified cross-sectional view of
the human body depicting one embodiment of
an implant configuration for the bone growth
stimulator depicted in FIGURES 1 and 2;

FIGURE 7 is a simplified isometric view of the
human body depicting one embodiment of an

implant configuration for the bone growth
stimulator depicted in FIGURE 3;

FIGURES 8a and 8b depict left and right halves
of a block diagram of the application specific
integrated circuit used in the bone growth
stimulator depicted in FIGURES 1 through 3;

FIGURE 9a is a graphical representation of the
communication protocol used by the circuit de-
picted in FIGURES 8a and 8b;

FIGURES 9b and 9c depict tables containing an
explanation of the down-link program data word
and up-link handshake, respectively, of the cir-
cuit depicted in FIGURES 8a and 8b;

FIGURE 10 illustrates a block diagram of the
crystal oscillator circuit depicted in FIGURE 8a;

FIGURE 11 illustrates a block diagram of the
power on reset circuit depicted in FIGURE 8a;

FIGURE 12 illustrates schematically the main
time base circuit depicted in FIGURE 8b;

FIGURE 13 illustrates a block diagram of the
output driver circuit depicted in FIGURE 8b;

FIGURE 14 illustrates schematically the trans-
mitter circuit depicted in FIGURE 8a;

FIGURES 15a and 15b illustrate schematically
the PPM decoder circuit depicted in FIGURE 8a;

FIGURE 16 illustrates a block diagram of the
communication modem circuit depicted in FIG-
URE 8b;

FIGURE 17 illustrates schematically the lead
status circuit depicted in FIGURE 8b;

FIGURE 18 illustrates schematically the receiver
circuit depicted in FIGURE 8a;

FIGURE 19 illustrates schematically the battery
status indicator circuit depicted in FIGURE 8b;

FIGURE 20 illustrates a block diagram of the
voltage reference/regulator circuit depicted in
FIGURE 8b;

FIGURE 21 illustrates schematically the circuit
depicted in FIGURES 8a and 8b configured for
the AC mode of operation; and

FIGURE 22 illustrates schematically the circuit
depicted in FIGURES 8a and 8b configured for
the DC mode of operation.

DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiment of the present in-
vention and its advantages are best understood by
referring to FIGURES 1 through 22 of the drawings,
like numerals being used for like and correspond-
ing parts of the various drawings.

The present invention will be described in con-
junction with the following Table of Contents:

- A. MECHANICAL PACKAGING
 - 1. AC Configuration
 - 2. DC Configuration
- B. OUTPUT CHARACTERISTICS

within the bone mass to be treated. Leads 34 are sheathed in a tube of elastomeric material.

In operation, DC stimulator 26 generates a DC current between cathodes 30 and anode 28. As will be described in connection with FIGURES 10 through 22, each cathode 30 of DC stimulator 26 is an independent current path.

B. OUTPUT CHARACTERISTICS

1. AC Configuration

FIGURE 4 is a graphical representation of the output of the bone growth stimulator depicted in FIGURES 1 and 2. AC stimulator 10 (depicted in FIGURES 1 and 2) generates an alternating current output. In the preferred embodiment, AC stimulator 10 generates an asymmetric output of 99 pulses (a "burst") followed by a rest period. After the rest period, the burst/rest cycle is repeated until AC stimulator 10 is turned off. The positive portion of the output pulse, indicated having the duration t_1 , is approximately $65\mu s$ long and has an amplitude of $900\mu A$. This current generates approximately $3mV/cm$ at the healing site in implantation configuration depicted in FIGURE 6. The negative portion of the output, indicated having the duration t_2 , is approximately $195\mu s$ long and has an amplitude of $-300\mu A$. Thus generates $-1mV/cm$ at the same healing site. The AC output signal is off after 99 pulses for approximately 640 milliseconds. The resulting burst/rest rate has a frequency of 1.49 Hz.

It should be understood that AC stimulator 10 may be made to output other wave forms, both symmetric and asymmetric. For instance, AC stimulator 10 could produce a wave form having a sinusoidal form. The amplitude of both the positive and negative portions of the output may be modified to provide a field strength of 0.3 to 3 mV/cm at the bone site. This range produces optimum healing results.

2. DC Configuration

FIGURE 5 is a graphical representation of the output of the bone growth stimulator depicted in FIGURE 3. DC stimulator 26 (shown in FIGURE 3) generates a constant negative current between its two cathodes and anode of approximately $-20\mu A$ during its operation.

3. IMPLANTATION CONFIGURATION

1. AC Configuration

FIGURE 6 is a simplified cross-sectional view of the human body depicting one embodiment of an implant configuration for AC stimulator 10.

stimulator 10 depicted in FIGURES 1 and 2. AC stimulator 10 is bisected along its longitudinal axis in a plane generally perpendicular to the planes containing the electrodes 14 and 16. AC stimulator 10 is implanted in the human body indicated generally by 36 near a vertebra 38. AC stimulator 10 is placed near vertebra 38 so that the electric field generated between electrodes 14 and 16 is made to penetrate a portion of vertebra 38 in need of bone growth stimulation. The outer limit of the electric field generated by AC stimulator 10 is indicated generally by field lines 40. Vertebra 38 typically is in need of bone growth stimulation when two or more vertebrae are clinically fused together.

Because of the AC nature and the electrode spacing of AC stimulator 10, vertebra 38 will receive the benefit of the electric field 40 even if AC stimulator 10 does not abut vertebra 38. For instance, AC stimulator 10 may be placed further than 1 centimeter away from the injured section of vertebra 38. This allows a surgeon to implant AC stimulator 10 subcutaneously. This simplifies implant and explant, reduces the chance of infection and improves imaging results. Imaging results are improved because there are no foreign objects near vertebra 38.

In the preferred embodiment, AC stimulator 10 is implanted subcutaneously with its electrodes 14 and 16 facing away from vertebra 38. Empirical studies have determined that this placement results in a better electric field distribution and lower inadvertent muscle stimulation.

2. DC Configuration

FIGURE 7 is a simplified isometric view of the human body depicting one embodiment of an implant configuration for the DC stimulator 26 depicted in FIGURE 3. Here, DC stimulator 26 is used to fuse a bone growth mass 42 to two adjacent vertebrae 38 of spine 44. DC stimulator 26 may be implanted subcutaneously. However, leads 34 must be inserted such that cathodes 30 (not shown) are directly in or adjacent to bone graft mass 42. It is not required that both cathodes 30 be placed at the same bone site.

It should be understood that both AC stimulator 10 and DC stimulator 26 may be implanted near any bone for the repair of several types of bone injuries. For instance, the stimulators may be used to promote bone healing in the long bones of the body. Also, the stimulators may be used at a bone site to promote the healing of a bone fracture.

cuit 68 is more fully described in connection with FIGURE 20.

2. Communications Protocol

FIGURE 9a is a graphical representation of the communication protocol used by the circuit depicted in FIGURES 8a and 8b. Integrated circuit 46 transmits and receives data at 1200 Hz. This rate results in a 833 μ s overall transmission window. After receiving a start pulse at the start window, integrated circuit 46 looks for the presence or absence of a data pulse in the "one window," "zero window" or "no pulse detected window." As depicted, these three data windows occur approximately 208 μ sec, 416 μ sec, and 624 μ sec after the start pulse. The communication protocol results in a data logic level one if a pulse is received in the one window and a data value zero if a pulse is received in the zero window. A communications error is indicated if a pulse is received in the no pulse detected window. The disclosed communications protocol permits additional error checking by requiring a pulse at both start windows and requiring one but not both of the one window and zero window to have a data value. Each window is approximately 104 μ s long. Data detection is enabled only in the four windows described above during each communication.

An external receiver/transmitter may be fabricated from a microprocessor with 1200 Baud capability connected to a suitable coil.

FIGURES 9b and 9c depict tables containing an explanation of the down-link program data word and up-link handshake respectively of the circuit depicted in FIGURES 8a and 8b. Integrated circuit 46 uses an 11 bit program data word. The down-link, or received data word comprises three programmable data bits. The second, third, and fourth bits of the down link program data word contain data which is used by integrated circuit 46 to adjust its mode of operation. Bit 2 is a read-not write (RNW) bit. When RNW equals zero, IC 46 acts upon the third and fourth bits as subsequently described. If RNW equals one, then IC 46 will simply up-link an 11 bit program data word to the external transmitter/receiver. The third and fourth bits, STIM0 and STIM1 indicate how long the bone growth stimulator runs. As depicted in FIGURE 9a, the bone growth stimulator has four modes of operation. (1) It may be continuously off. (2) It may be on 4 hours, off 20 hours. (3) It may be on 8 hours, off 16 hours. (4) It may operate continuously. All other bits in the down link program data word do not vary. The first, sixth, and seventh bits must be a logic 1 while the fifth, eighth, and eleventh bits must be a 0. The ninth and tenth bits must follow the hard-wired control bits DCON and CODE

spectively. DCON is an externally hard-wired bit indicating whether the bone growth stimulator is configured for AC or DC output. A logical level of 0 indicates an AC output while a logic level of 1 indicates a DC output. CODE is an externally hard-wired input bit. It may be used, for instance, to indicate a first and second version of manufactured stimulators. The down-link program data word is transmitted left to right.

The up-link program data word transmitted from integrated circuit 46 to an external receiver has 8 bits of data, an odd parity check, and start and stop bits. The start and stop bits are logic high and low respectively. The second and third bits indicate the present mode of operation of IC 46 as described in connection with the down-link program data word. The fourth and fifth bits indicate whether the DCON or CODEs bits are high or low. The sixth and seventh bits indicate the status of the stimulator leads. In the AC mode, these bits indicate whether electrode 16 (shown in FIGURES 1 and 2) is normal, has a low impedance or has a high impedance. In the DC mode, these bits indicate whether either of leads 34 (shown in FIGURE 3) has an abnormally high impedance. The particular logic values for each condition in each mode is defined in this FIGURE. The eighth and ninth bits indicate the status of the internal battery of the bone growth stimulator. The battery status circuitry 62 (depicted in FIGURE 8) monitors the battery voltage for two trippoints, 2.1 V and 2.4 V. These voltages correspond to the end of life (EOL) and low battery (LOWBATT) depicted as indicated in the FIGURE. The tenth data bit is an odd parity check bit. It is high when the number of ones preceding it is even and it is low when the number of ones preceding it is odd.

3. Signal/External Input Description

The following signals are used by integrated circuit 46 internally and as external connections:

ANL_CLK is generated by main time base circuit 52. It enables lead status circuit 62 during certain intervals of the DC output signal.

BIASON is generated by the main time base circuit 52. In the AC mode, it turns on the bias current for the positive portion of the output signal. It is disabled during the negative portion of the AC signal output. In the DC mode, it is continuously high. BIASON is used by the output driver.

C1_49 is generated by main time-base circuit 52. It is a clock signal of 1.49 Hz. It is used as a gating signal for the control logic of the output switches of output driver 54.

C76_8 is generated by crystal oscillator circuit 48. It is a clock signal of 76.8 kHz. It is the main

NRESET is generated by power on reset circuit 50. It is reset on power up and after a valid downlink/uplink communication. In either case, it returns high after two 76.8 kHz clock cycles.

NRST is generated by power on reset circuit 50. It is reset on power up and after a valid downlink/uplink communication. In either case, it returns to its high state after one 1.49 Hz clock cycle.

NRSTPRG is generated by power on reset circuit 50. It is reset on power up. It returns to its high state after NRST transitions high.

NSTRT is generated by communication modem circuit 60. It initiates a reset after a valid downlink/uplink communication.

NTRANS is generated by communication modem circuit 60. It indicates the completion of a valid downlink communication.

NTRANS_OUT is generated by transmitter unit 58. It is the output signal of the driver stage of the transmitter circuit 56. It is connected to an external coil (Pad 8).

ONECLK is generated by PPM decoder circuit 58. It is the decoded clock signal corresponding to the data position for logic level one in the communications protocol.

OUT1 is an output from output driver circuit 54 (Pad 23). In the both the AC and DC modes, this is the output signal.

OUT2 is an output from output driver circuit 54 (Pad 24). In the AC mode, OUT2 is connected to OUT1. In the DC mode, OUT2 is the second independent current path.

REC_OFF is generated by PPM decoder circuit 58. This signal disables the receiver, battery status and output driver circuits during an uplink operation.

RECV is input to receiver unit 56. It is coupled to an external coil (Pad 9).

STARTCLK is generated by PPM decoder circuit 58. It is a decoded clock signal corresponding to the start position in the communications protocol.

STIM0 is generated by communication modem circuit 60. It is used with the STIM1 bit to generate the four stimulation modes (off, on 4 hours, on 4 hours, on continuously).

STIM1 is generated by communication modem circuit 60. It is used with the STIM0 signal to generate the four stimulation modes (off, on 4 hours, on 8 hours, on continuously).

SYMTRM is an input to output driver circuit 54. It may be coupled to GND_REF or V_{DD} through an external resistor (Pad 21). It is used to trim the positive portion of the output current. It is presently not used.

TCODE is generated by communication

transmitter circuit 56 for external transmission.

TEST is a testing signal used in conjunction with TP1 through TP6. It is brought off chip at pad 4.

TP1 through TP6 are external test points (Pads 26, 27, 28, 1, 2, and 3 respectively). They output data from the various cell blocks for testing purposes.

V_{DD} is an external connection to the positive terminal of the 2.8 V battery (Pad 14).

V_{SS} is an external connection to the negative terminal of the 2.8 V battery (Pad 11).

VREF is an input to voltage reference/regulator circuit 68. It is coupled to a 1.5 V unbuffered reference voltage (Pad 17).

VSET1 is an input to voltage reference/regulator circuit 68. It is coupled to V_{DD} through two external resistors in series (Pad 15). It is used to trim VREF.

VSET2 is an input to voltage reference/regulator circuit 68. It is coupled to V_{DD} through a resistor (Pad 16). It is also used to trim VREF.

XMIT is generated by communication modem circuit 60. It enables the transmitter output.

XTAL1 is an external connection to one terminal of a 76.8 kHz oscillator/resistor circuit (Pad 6). It is an input to crystal oscillator circuit 48.

XTAL2 is an external connection to one terminal of a 76.8 kHz oscillator/resistor pair (Pad 7). It is an input to crystal oscillator circuit 48.

XTRM is an external connection to V_{DD} through a resistor (Pad 5). It sets the bias current on the 76.8 kHz crystal oscillator.

ZEROCLK is generated by PPM decoder circuit 58. It is the decoded clock signal corresponding to a logic level zero in the communications protocol.

4. Circuit Description

a. Crystal Oscillator

FIGURE 10 illustrates a block diagram of the crystal oscillator circuit 48 depicted in FIGURE 8a. Crystal oscillator circuit 48 comprises a crystal driver 70, a hysteresis comparator 72, and an output driver 74. Crystal driver 70 is connected to crystal X1 and resistor R2 through pads 6 and 7. Crystal X1 and resistor R2 are themselves connected in parallel. The inputs of hysteresis comparator 72 are also coupled to crystal X1 and resistor R2 through pads 6 and 7. The output of hysteresis comparator 72 is connected to output driver 74 which outputs signal C76_8. An external resistor R1 is coupled between V_{DD} and pad 5. Pad 5 is coupled to two current sources 76 and 78 in

alternate output (PW) of divide-by circuit 106. Output PW, labeled CLK2, generates a pulse identical to the output of divide-by circuit 106 occurring on the falling edge of the output of divide-by circuit 106. NRESET and REC_OFF are input to an AND/NAND gate 126 after REC_OFF is inverted by an inverter 128. The nanded output of gate 126 is combined with DCON by a NOR gate 130. The output of gate 130 is connected to the RESET input of flipflop 122. The ANDed output of gate 126 is connected to the reset input of a D-type flipflops 132 and 134. Flipflop 132 has as its input the output of an AND gate 136. Gate 136 has two inputs, STIM_ON (the output of divide-by circuit 116) and the output from divide-by circuit 110. The input to flipflop 134 is connected to the output of an AND gate 138. Gate 138 has as its two inputs STIM_ON and the output from an OR gate 140. OR gate 140 has two inputs, DCON and the output from divide-by circuit 110.

ANL_CLK is the output from a three input AND gate 142. Gate 142 has inputs DCON, the output of gate 136 and the output of flipflop 132. NEN_ANL is generated from the output of an OR gate 144 inverted by an inverter 146. OR gate 144 has inputs which are the outputs of gate 136 and flipflop 132. NOUT_ON is generated by the output of an OR gate 148 inverted by an inverter 150. Gate 148 has inputs which are the outputs of OR gate 144 and of an AND gate 152. Gate 152 has two inputs STIM_ON and DCON. IMINUS2 is generated from the output of an OR gate 154 inverted by an inverter 156. Gate 154 has inputs which are the outputs of flipflop 134 (inverted) and gate 130. IMINUS is generated from the output of an OR gate 158 inverted by an inverter 160. Gate 158 has inputs which are the outputs of flipflop 134 (inverted) and flipflop 122. NIPLUS is generated from the ANDed output of a dual AND/NAND gate 162 inverted by an inverter 164. Gate 162 has as its inputs the outputs from flipflops 122 and 134. BIASON is generated by the output of an AND gate 166 inverted by inverter 168. Gate 166 has as its input the nanded output of gate 162 and DCON inverted by an inverter 170.

In addition, T-gates 172 and 174 have their outputs coupled to TP1. The input of T-gates 172 and 174 are coupled to the alternate output, PW, of divide-by circuit 106 and the output of flipflop 134, respectively. T-gates 172 and 174 are controlled by TEST. When TEST equals 0, TP1 is connected to output PW of divide-by circuit 106. When TEST equals 1, TP1 is connected to the output of flipflop 134.

In operation, the output of divide-by circuit 116 (STIM_ON) generates a series of four-hour PULSES depending upon the values of STIM1 and

= 0 and STIM0 = 0, then STIM_ON is low continuously, if STIM1 = 0 and STIM0 = 1 then STIM_ON is periodically high for 4 hours and low for 20, if STIM1 = 1 and STIM0 = 0, then STIM_ON is periodically high for 8 hours and low for 16, if STIM1 = 1 and STIM0 = 1, then STIM_ON is continuously high. This internal signal controls the four modes of operation of the stimulator. The output of divide-by circuit 104 acts as the timing clock for main time base circuit 52. The alternate output, PW, of divide-by circuit 106 generates the 25% high/75% low duty cycle in the AC mode. Divide-by circuit 108 generates 99 PULSES for each burst of the AC signal. Divide-by circuit 110 generates the burst to rest ratio of 1:25. This is the 1.49 Hz output in the AC mode.

The final divide-by operations are split among three divide-by circuits 112, 114 and 166 to facilitate testing. This allows main time base circuit 52 to be tested using an artificial 20-second day. As described above, when TEST = 1 the divide-by circuit 114 is bypassed. Also, as described above, the output of divide-by circuit 106 and flipflop 134 may be viewed directly through T-gates 172 and 174 through TP1.

d. Output Driver

FIGURE 13 illustrates a block diagram of the output driver circuit 54 depicted in FIGURE 8b. Output driver 54 comprises current mirrors 176, 178, 180, 182, 184, 186, and 188. Current mirror 176 is connected to V_{DD} through pad 25 and an external resistor R11. Current mirror 176 has a control voltage input, GND_REF. Current mirror 176 is connected to current mirror 178 through a switch 190. Switch 190 is controlled by NOUT_ON. Current mirror 178 mirror is connected between switch 190 and V_{SS}. Current mirror 180 is connected between V_{DD} and node 192. Node 192 is connected to V_{DD} also through an optional external resistor R12 at pad 21. Node 192 is also connected to current mirror 182 through a switch 194. Switch 194 is controlled by BIASON. Current mirror 182 is also connected to V_{SS}. Current mirror 184 is connected between V_{DD} and a node 196. Node 196 is connected externally to ILIMIT, at pad 22. Node 196 is also coupled to a node 198 through a switch 200. Switch 200 is controlled by NIPLUS. Node 198 is connected externally to OUT1, at pad 23 and to control mirror 186 through a switch 202. Switch 202 is controlled by IMINUS. Control mirror 186 is also connected to V_{SS}. A switch 204 is controlled by IMINUS2 and connects an external output, OUT2, at pad 24 to current mirror 188. Current mirror 188 is also connected to V_{SS}.

Resistor R11 trims the current through current

of the inverted output of flipflop 258, DSTB and the output of a NAND gate 254. The set input to flipflop 242 is connected to the output of a NAND gate 268. The inputs to NAND gate 268 are connected to the output of inverter 250 and to NPPMRST through an inverter 270.

T-gates 272 and 274, alternately switch REC_OUT and TELCLK to TP4 under control of TEST. When TEST equals zero, TP4 is connected to the 4800 Hz signal TELCLK. When TEST equals one TP4 is connected to REC_OUT.

In operation, flipflops 240, 242, 244, 246 and 248 capture data present on NREC_OUT which is synchronized with the 4800 Hz TELCLK signal. Gate 254 ensures that the data bit follows the PPM protocol described in connection with FIGURE 9a. Gate 254 outputs a high signal if any of the three PPM conditions are not met: (1) the start bit is high, (2) either the second or third bit is high, but not both or neither and (3) the no pulse detected window is low. Flipflop 258 and inverter 260 generate REC_OFF.

FIGURE 15b illustrates a schematic diagram of PPM clock decode block 238 depicted in FIGURE 15a. Block 238 comprises six D-type flipflops 276, 278, 280, 282, 284 and 286. These flipflops are cascaded together such that the output of flipflops 276, 278, 280, 282 and 284 are connected to the clock input of flipflops 278, 280, 282, 284 and 286, respectively. The clock input to flipflop 276 is connected to the output of AND gate 288. Gate 288 has two inputs, C76_8 and the output of an AND gate 290. AND gate 290 has inputs NSTOP and NTRANS. The output gate 290 is also connected to the resets of flipflops 276, 278 and to a D-type flipflop 292. Flipflop 292 is clocked by the output of flipflop 278 and its input is held high by V_{DD}. The output of flipflop 292 generates the signal NPPMRST. The inverted output of flipflop 292 inverted by an inverter 294 resets flipflops 280, 282, 284 and 286.

The input and inverted output of each of flipflops 276, 278, 280, and 282 are tied together to form nodes 296, 298, 300, and 302. These nodes form the inputs to OR gate 304. ZEROCLK is generated by a NOR gate 306. Gate 306 has three inputs, the output of gate 304, a node 308 and the output of flipflop 286. Node 308 is connected to the input and inverted output of flipflop 284. ONECLK is generated by a NOR gate 310. Gate 310 has three inputs, the output of gate 304, the output of flipflop 284 and the output of latch 286. STARTCLK is generated by a NOR gate 312. NOR gate 312 has three inputs, the output of gate 304, node 308 and the inverted output of flipflop 286. DSTB is generated by a NOR gate 314. NOR gate 314 has four inputs, node 300, the output of flipflop 282,

to the input and the inverted output of flipflop 286. TELCLK is generated from node 302 inverted by an inverter 316.

g. Communications Modem

FIGURE 16 illustrates a block diagram of the communication modem circuit 60 depicted in FIGURE 8b. Communication modem circuit 60 comprises an 11 bit shift register 318 with outputs NSTRT and an 11 bit bus 320. Shift register 318 is reset by NPPMRST and is clocked by DSTB. DATA and REC_OFF are logically combined by an OR gate 322. The output of gate 322 is the data input to shift register 318. Bus 320 connects shift register 318 to protocol check circuit 324, to 11-to-1 multiplexer 326 and to stimulation control bit latches 328.

Protocol check circuit 324 has inputs DCON, CODE through pads 13 and 10, respectively. Protocol check circuit 324 has a single output ACCESS input to latches 328 and to a downlink/uplink control circuit 330. Latches 328 also have inputs NRSTPRG, DCON, and the output from circuit 330. Latches 328 output STIM0 and STIM1. Circuit 330 also has inputs NPPMRST and C38_4. As depicted, multiplexer 326 has data inputs STIM0, STIM1, DCON, CODE, LDLOW, LDHIGH, LOWBATT, and EOL. Multiplexer 326 also has two control inputs STARTCLK and REC_OFF. Multiplexer 326 outputs TCODE and XMIT.

A switch 332 alternately switches an external connection, TP5, to either the tenth data line in bus 320 or to ACCESS depending upon the logic value of TEST. If TEST = 0, then TP5 is connected to ACCESS. If TEST = 1, TP5 is connected to a data line within bus 320 containing the final or stop bit of information. Pad 2 is connected to TP5 while pad 4 is connected to TEST.

In operation, 11 bits of data are strobed into shift register 318 through DSTB and DATA. These bits are then made available on bus 320. Protocol check circuit 324 then compares the received data with the programmed data word requirements described in connection with FIGURE 9b. If these requirements are met, then protocol check circuit 324 outputs a logic one on ACCESS. Latches 328 check the second received data bit to determine if STIM0 and STIM1 should be written to (RNW = 0) or simply read from (RNW = 1). If a write command is indicated on bus 320, latches 328 will be loaded with new data. If only a read operation is indicated, communication modem 60 will uplink a handshake communication to the external receiver. Circuit 330 outputs a logic zero on NTRANS after a valid communication is received as indicated by protocol check circuit 324.

has a capacitance of 1000 pF.

In operation, comparator 368 pulses low when inductor L1 receives a pulse from an external transmitter. Comparator 368 can detect a pulse of approximately 20 mV in amplitude, 7.5 μ sec in width, and pulses spaced as close together as 75 μ sec.

j. Battery Status Indicator

FIGURE 19 illustrates schematically the battery status indicator circuit 66 depicted in FIGURE 8b. Battery status circuit 66 comprises a comparator 376. The output from comparator 376 is logically combined with REC_OFF by an AND gate 378. The output of gate 378 is connected to the input of a latch 380. Latch 380 is reset by NRST and its output generates LOWBATT. The output of latch 380 is combined with the output from gate 378 by an AND gate 382. The output of AND gate 382 is connected to the input of a latch 384. Latch 384 is reset by NRST and clocked by C1_49. Latch 384 requires two clock cycles to latch. The output of latch 384 generates EOL.

The first input to comparator 376 is connected to a node 386. Node 386 is connected to an external node 388 through EOLTRM and pad 12. External capacitor C3 is connected between node 388 and V_{DD}. An external resistor R4 is connected between the node 388 and V_{SS}. Two current mirrors 390 and 392 are connected in parallel between node 386 and a node 394. A switch 396 selectively connects current source 392 to node 394 under control of the output of latch 380. Node 394 is coupled to V_{DD} by a switch 398 under control of NEN_ANL. The second input of comparator 376 is connected to GND_REF.

A switch 400 alternately connects TP3 through pad 28 to either the output of gate 378 or the output of latch 384. Switch 400 is controlled by TEST through external pad 4. When TEST equals zero, TP3 is connected to the output of gate 378. When TEST equals one, TP3 is connected to the output of latch 384.

In operation, comparator 376 compares the voltage at node 386 with GND_REF. The first voltage, that of node 386, is constant depending upon how much current is drawn through resistor R4 by current mirrors 390 and 392. GND_REF however drops as V_{DD} drops during the lifetime of the circuit.

Initially, the output of latch 380 is low and switch 396 is closed. Current mirrors 390 and 392 sink 120 nA through resistor R4. Initially, GND_REF is at a higher potential than node 386. The output of comparator 376 is therefore low. As the battery ages, GND_REF will drop below the constant voltage at node 386 and trip the output of

bit from latch 380 and open switch 396. Node 386 will therefore only have 80 nA current flowing through it. This will lower the voltage of node 386. GND_REF will again be higher than the voltage at node 386 causing output of comparator 376 to go low again. Eventually as the battery continues to age, GND_REF will drop below the second, even lower, voltage level at node 386 tripping the output of comparator 376 high. The second high output will be combined with the output from latch 380 by gate 382 and output as EOL.

k. Voltage Reference/Regulator

FIGURE 20 illustrates a block diagram of the voltage reference/regulator circuit 68 depicted in FIGURE 8b. Voltage reference/regulator circuit 68 comprises a diode 403 connected to V_{DD} and node 402, biased as depicted. Node 402 is connected to V_{SS} through a current mirror 404. A second diode 405 is connected between V_{DD} and VSET1 through pad 15. VSET1 is coupled to VSET2 through external resistor R5. VSET2 exits the circuit through pad 16. VSET2 is coupled to a node 406. Node 406 is coupled to V_{SS} through a current mirror 408. An op-amp 410 has its first input to node 406 and its second input connected to node 402. An external resistor R6 is connected between V_{DD} and pad 16. External resistor R7 is connected between V_{DD} and a node 412. Node 412 is coupled to VREF through pad 17. Pad 17 is connected to V_{SS} through a current mirror 414. Node 412 is the first input of comparator 416. The second input to comparator 416 is tied to its output. The output of comparator 416 generates GND_REF (internally and GND externally). GND_REF is coupled to one terminal of an external capacitor C5 through external pad 18. The second terminal of capacitor C5 is coupled to V_{DD}. First and second current mirrors 418 and 420 are connected in series between V_{DD} and V_{SS}. Current mirrors 422 and 424 are coupled to V_{DD} and generate the 20 nA bias currents IREC and ILEAD respectively. ITEST is connected to V_{SS} through a current mirror 426. IDCON is connected to V_{SS} through a current mirror 428. ICODE is connected to V_{SS} through a current mirror 432. IPOR is connected to V_{SS} through a current mirror 434. Current mirrors 426, 428, and 430 generate 100 nA bias currents. Current mirrors 432 and 434 generate a 20 and 10 nA bias current respectively.

NRSTPRG controls a switch 436. Switch 436 connects V_{DD} to a current mirror 438. The output of voltage mirror 438 is connected to output of comparator 410. The currents flowing through current mirrors 438, 404, 408, 414, 420, 426, 428, 430, 432

D2 and capacitor C7 are connected in parallel between OUT1 and ILIMIT. ILIMIT is connected to the anode, CAN.

Certain resistors and capacitors may have different values to reflect the DC configuration. This adjustment can be made by one skilled in art in connection with the foregoing description.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

Claims

1. A method for the therapeutic stimulation of bone growth of a bone site comprising the steps of:
 - implanting first and second electrodes into the tissue near the site, the first and second electrodes coupled to a bone growth stimulator; and
 - generating an alternating current between the first and second electrodes using the bone growth stimulator.
2. An implantable bone growth stimulator comprising:
 - first and second electrodes for being implanted adjacent a bone site; and
 - circuitry for generating an alternating current between said first and second electrodes, said alternating current operative to stimulate bone growth at the bone site.
3. The stimulator of Claim 2 wherein said circuitry for generating further comprises circuitry for generating an asymmetric alternating current.
4. The stimulator of Claim 2 wherein said circuitry for generating further comprises circuitry for generating a symmetric alternating current.
5. The stimulator of Claim 2 further comprising:
 - circuitry for receiving signals transmitted external to the stimulator, the signals representative of a desired mode of operation of the stimulator; and
 - circuitry for modifying the mode of operation of the stimulator responsive to the external signals.
6. The stimulator of Claim 5 wherein said circuitry for modifying further comprises circuitry for modifying the duration of time the stimulator generates the alternating current.
7. The stimulator of Claim 2 further comprising:
 - circuitry for monitoring the status of the stimulator; and
 - circuitry for generating signals representative of the status of the stimulator and transmitting the signals to a receiver external to the stimulator.
8. The stimulator of Claim 7 wherein said circuitry for monitoring comprises circuitry for monitoring the voltage drop across a battery within the stimulator.
9. The stimulator of Claim 7 wherein said circuitry for monitoring further comprises circuitry for monitoring the voltage of one of said electrodes.
10. The stimulator of Claim 7 wherein said circuitry for monitoring further comprises circuitry for monitoring the duration that said circuitry for generating outputs the alternating current.
11. The stimulator of Claim 2 further comprising a spacing mechanism for generally maintaining a predetermined distance between said first and second electrodes.
12. The stimulator of Claim 2 wherein said spacing mechanism comprises a thin elongate member of elastomer.
13. The stimulator of Claim 12 wherein said thin elongate member further comprises silicon.
14. The stimulator of Claim 12 wherein said thin elongate member further comprises urethane.
15. The stimulator of Claim 12 wherein said thin elongate member further comprises silicon-urethane.

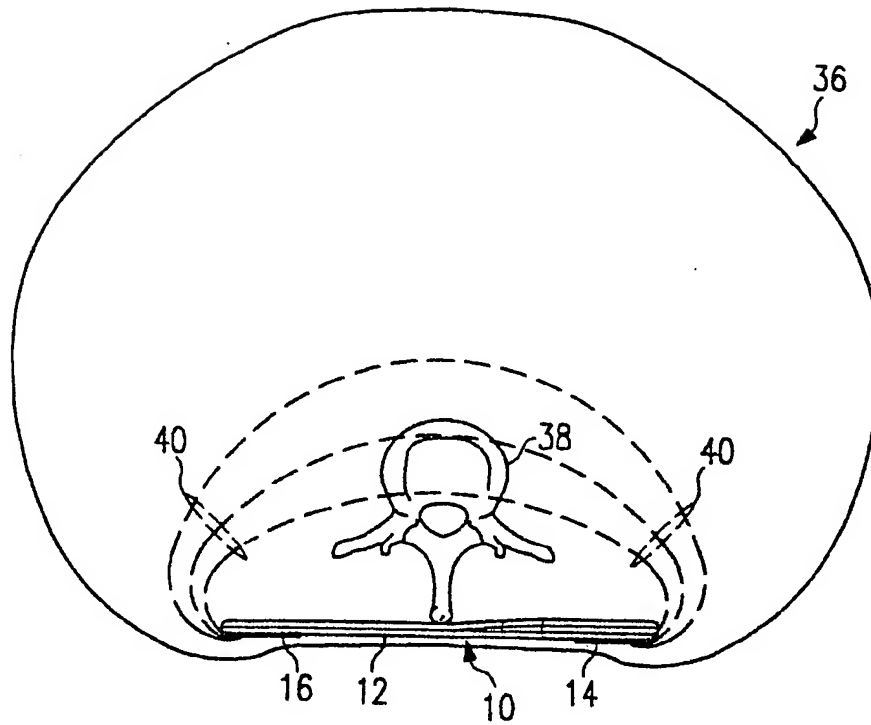


FIG. 6

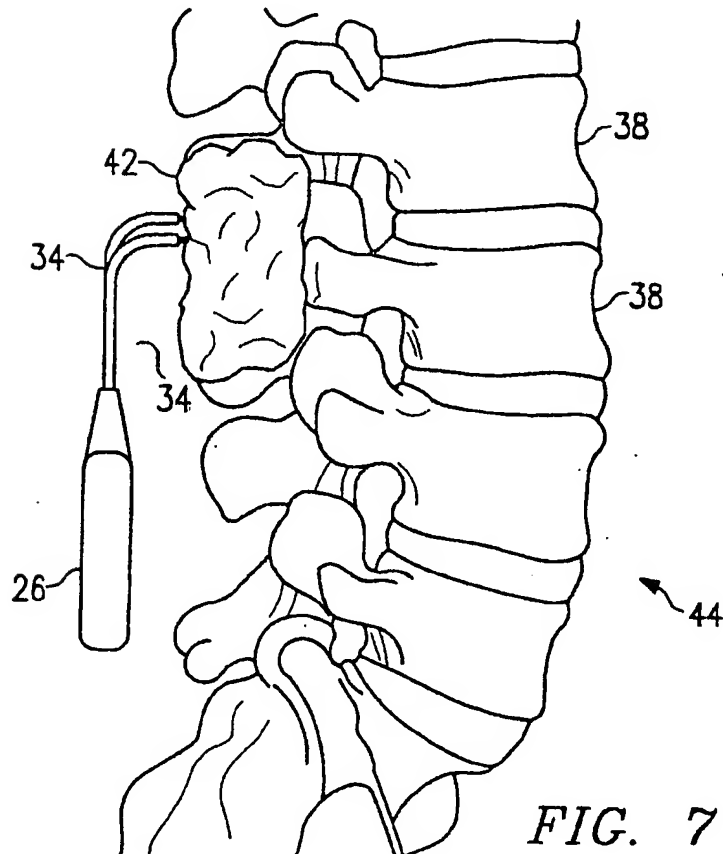


FIG. 7

FIG. 8b

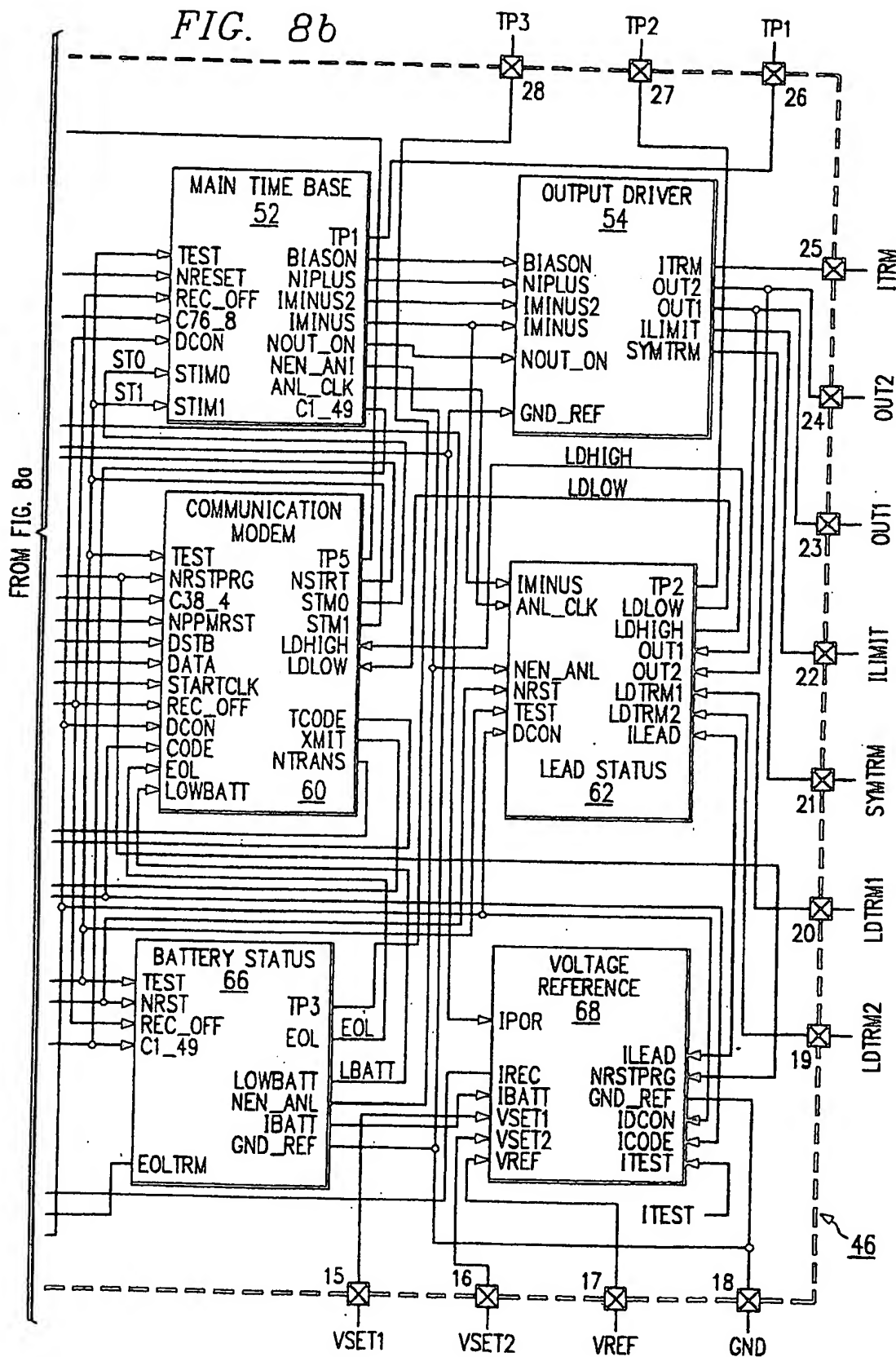
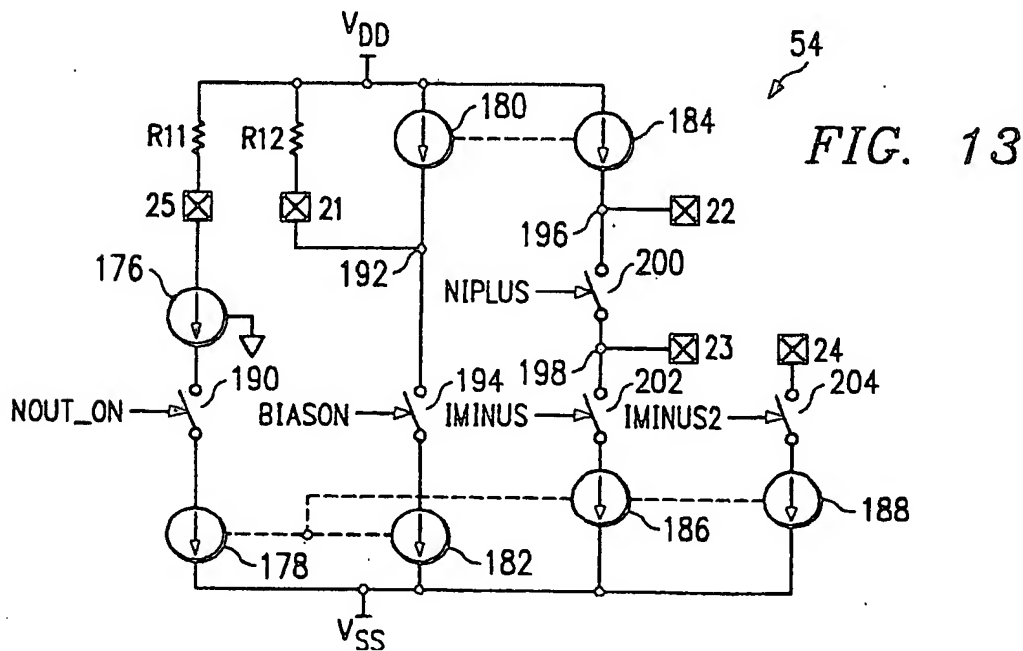
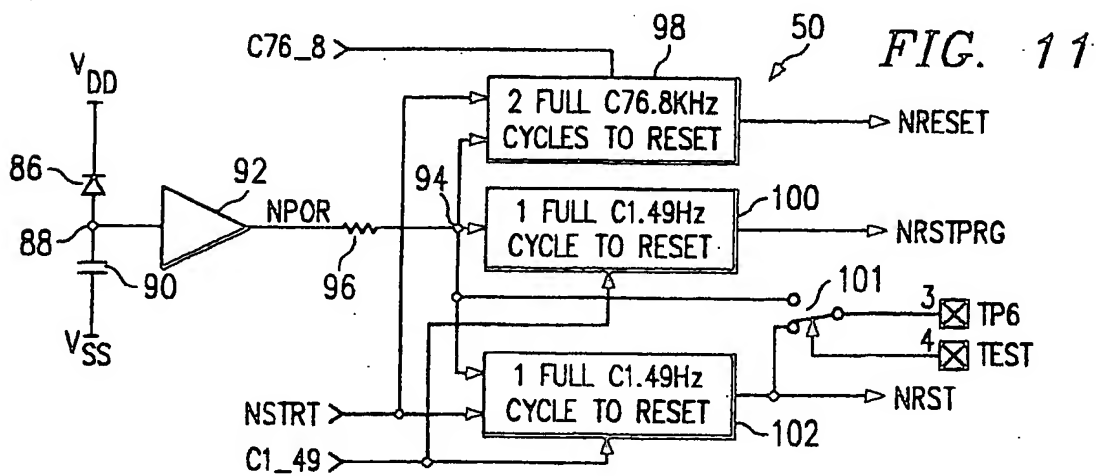
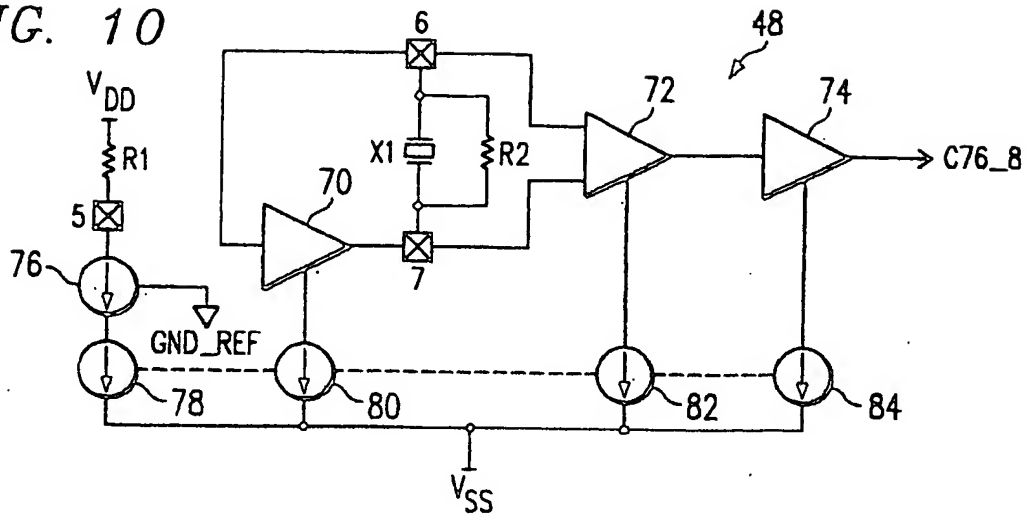
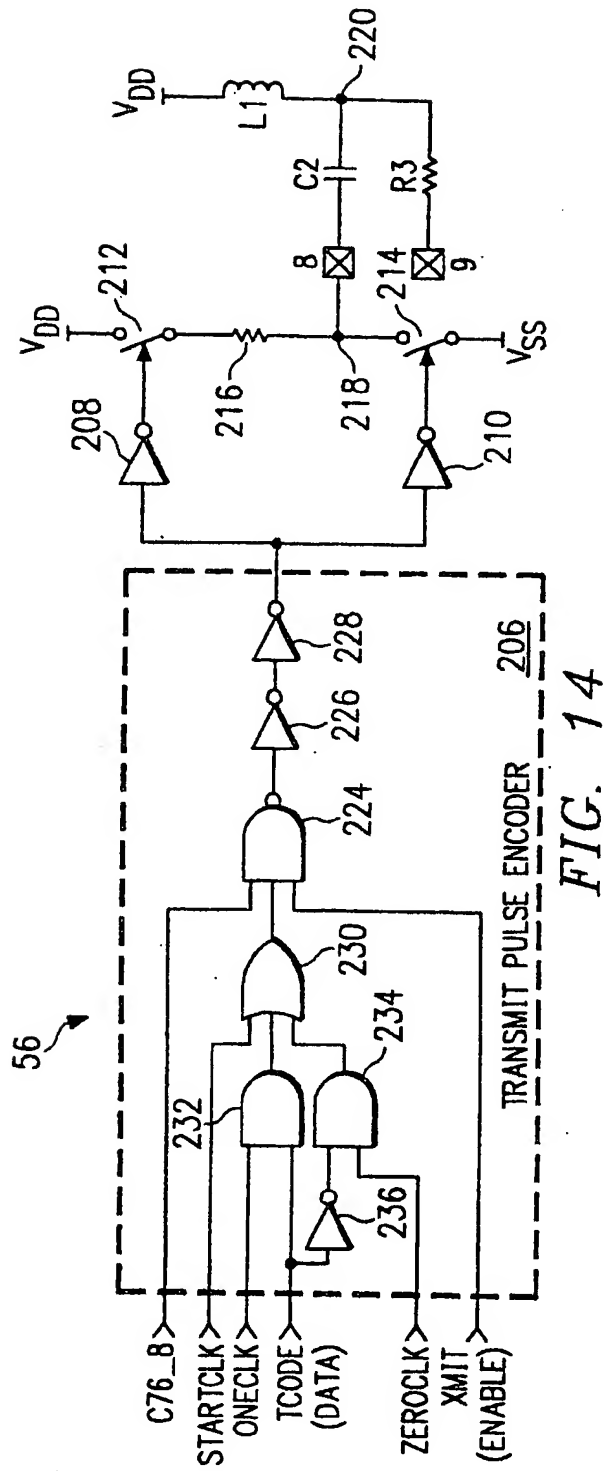
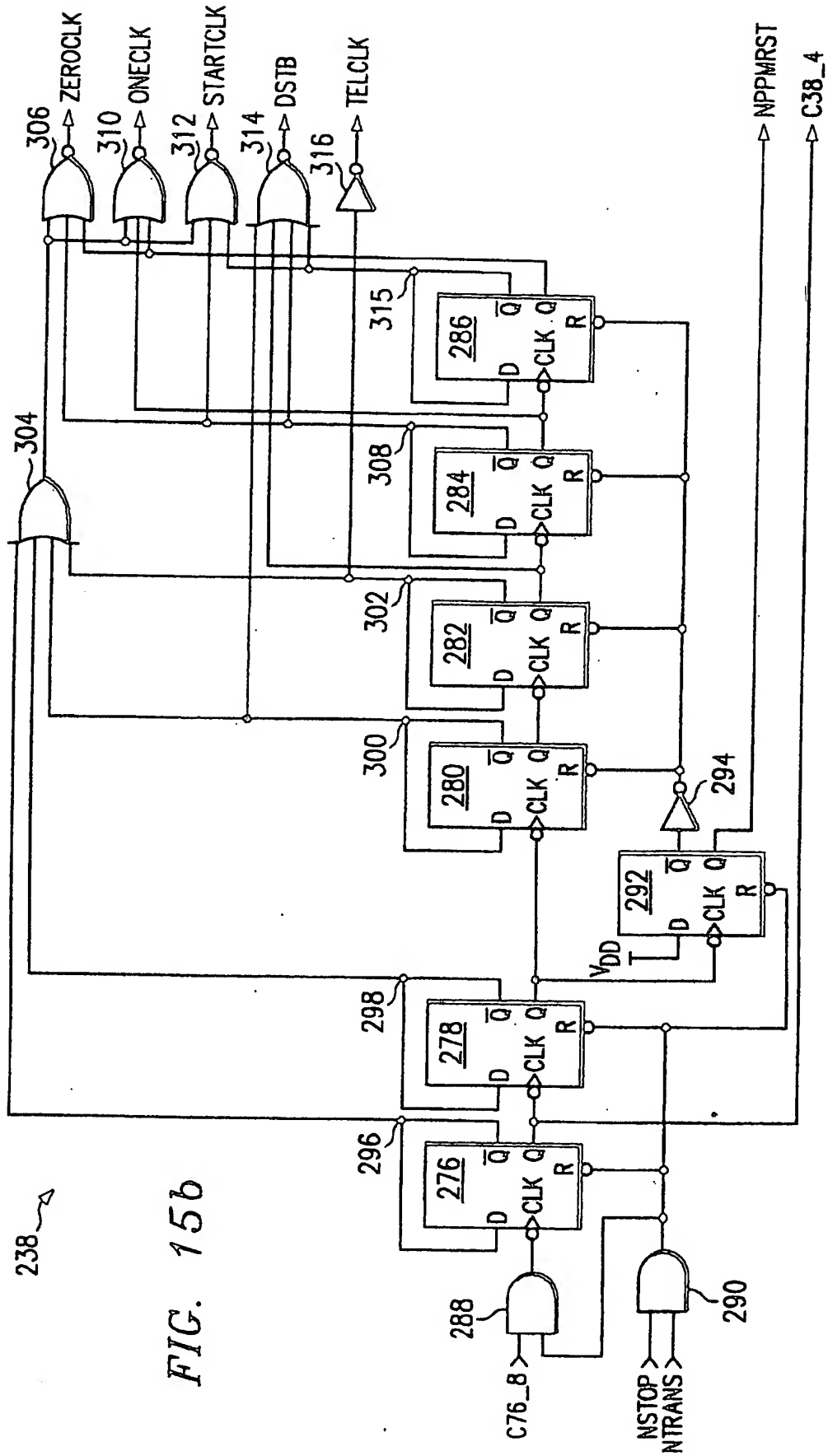
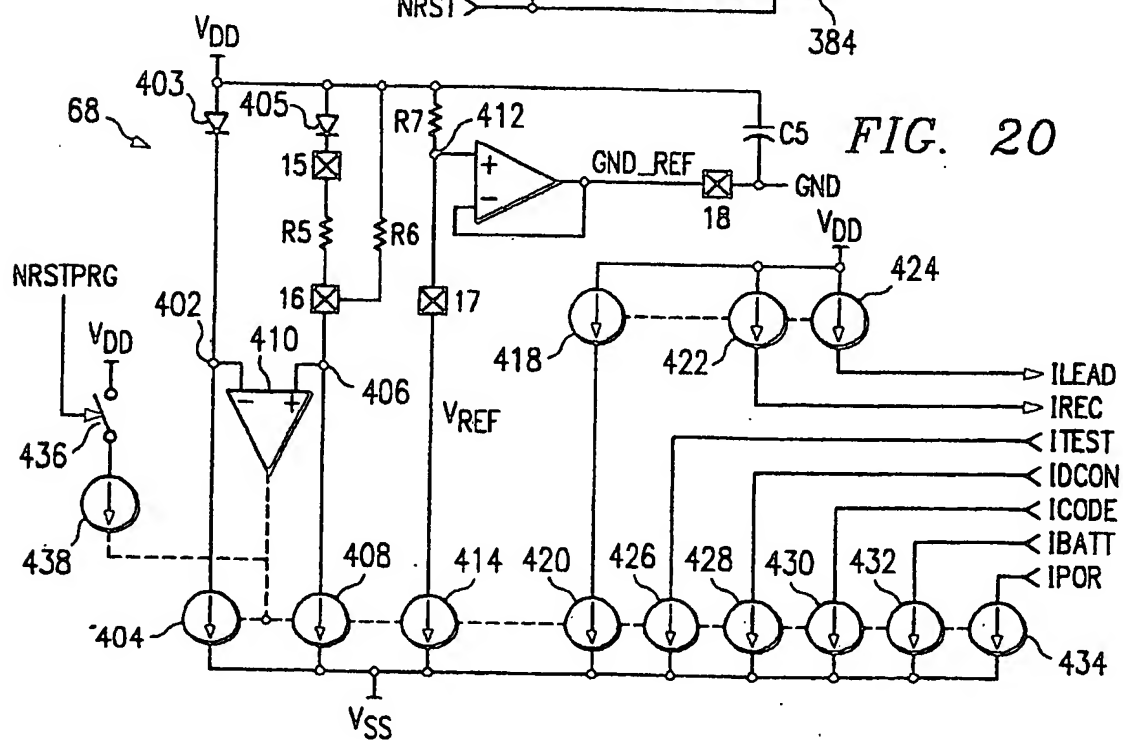
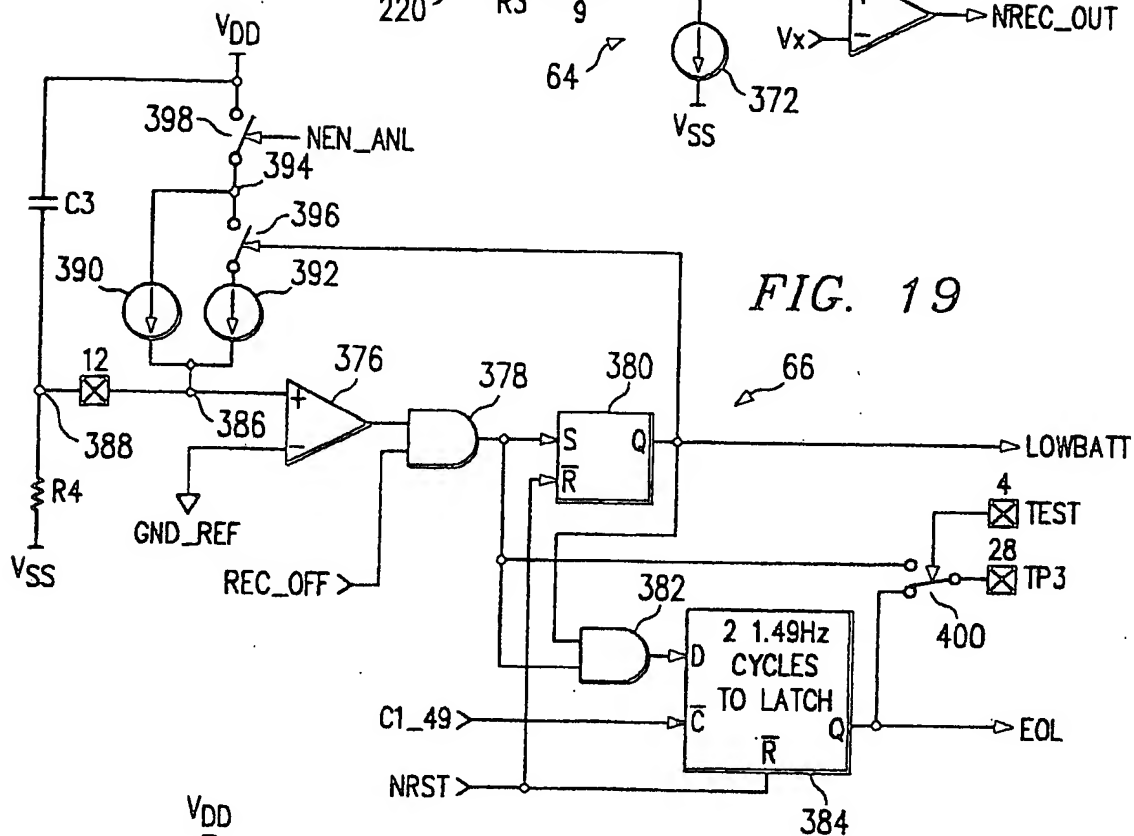
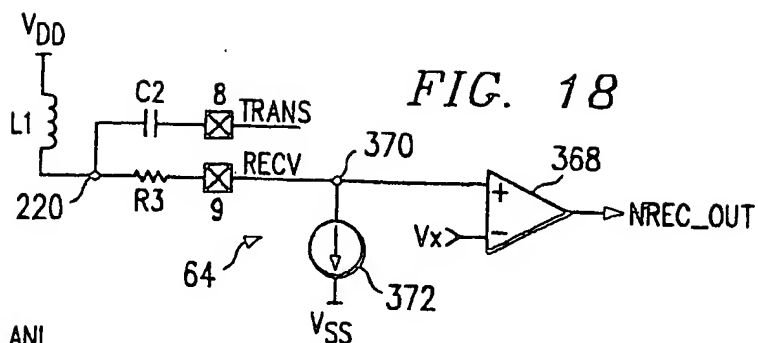


FIG. 10









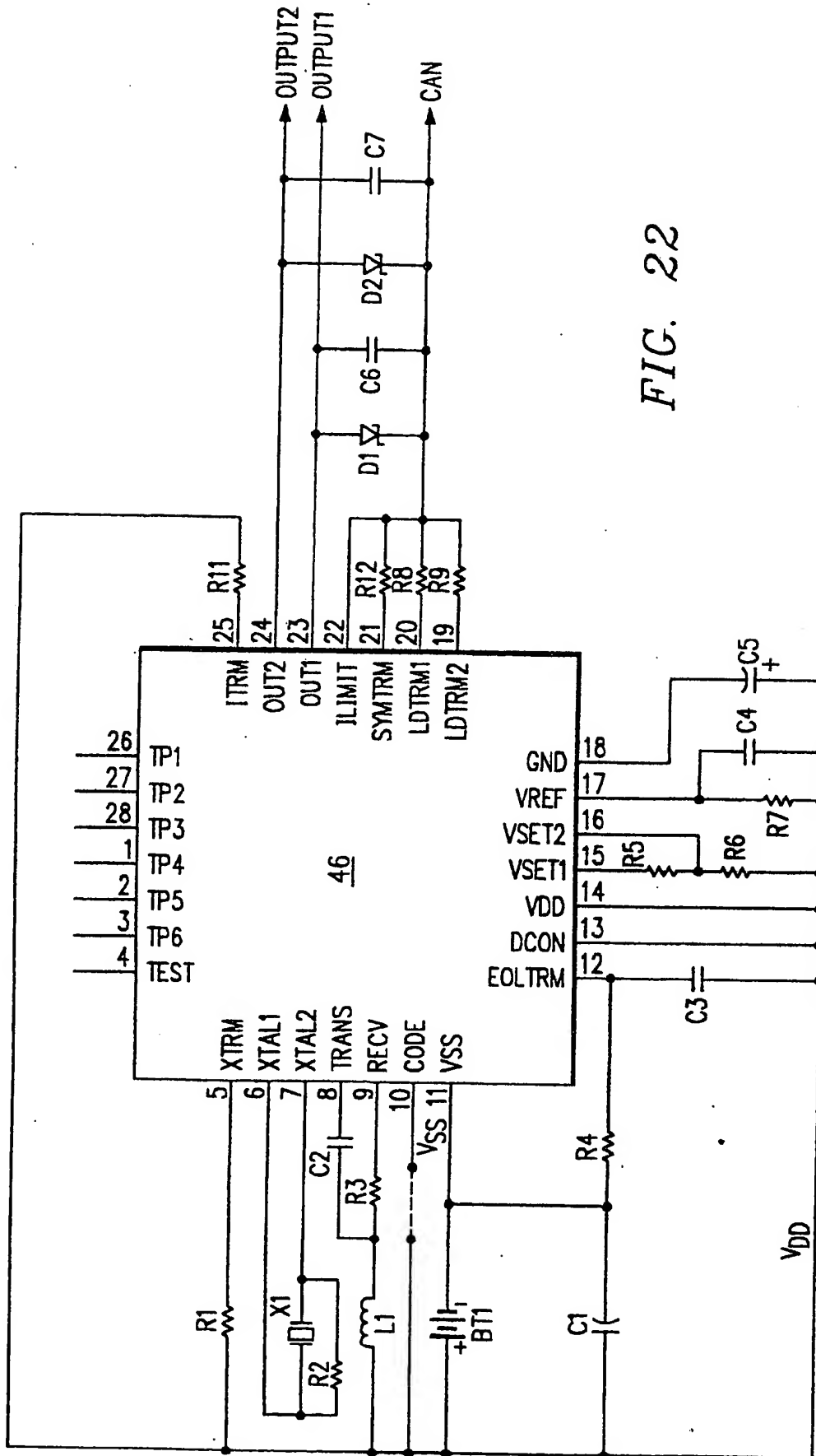


FIG. 22

(19)



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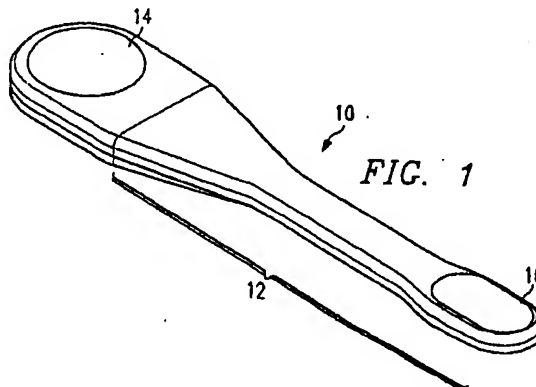
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(54) Implantable bone growth stimulator and method of operation.

(57) A method for the therapeutic stimulation of bone growth of a bone site is disclosed comprising the steps of implanting first and second electrodes (14,16) into the tissue near the base site. The electrodes (14,16) are coupled to a bone growth stimulator (10) which generates an alternating current.



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INCOMPLETE SEARCH

Claims searched completely: 2-15

Claim not searched: 1

Method for treatment of the human or
animal body by surgery or therapy
(see article 52(4) of the European
Patent Convention)